

ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device includes fuse cells arranged at a fuse cell array, a fuse cell data program and erase circuit, a fuse cell data control circuit, and fuse data latch circuits. The fuse cells include erasable and programmable nonvolatile memory cells. The fuse cell data program and erase circuit programs fuse data to the memory cells and erases the fuse data from the memory cells. The fuse cell data control circuit controls read out timing of the fuse data stored in the memory cells based on a signal generated upon detection of power-on. The fuse data latch circuits latch the fuse data read out from the memory cells.